WHAT IS CLAIMED IS:

1. A method for manufacturing a memory device, comprising:

forming a first oxide layer on top of a substrate;

forming a gate layer on top of the first oxide layer;

forming a second oxide layer over the gate layer;

removing a portion of the second oxide layer and the gate layer to form a first opening in the second oxide layer and a second opening in the gate layer, the first and second openings exposing a portion of the first oxide underneath the gate layer, the width of second opening being bigger than the width of the narrowest region of the first opening in the second oxide layer so that the gate layer is pulled back horizontally underneath the second oxide layer;

forming a source region in the substrate underneath the first oxide layer;

forming a third oxide layer in the first and second openings, the third oxide layer conforming to a contour thereof;

removing a portion of the third oxide layer and the first oxide layer to make a third opening; and

depositing a control gate material in the third opening.

2. The method of claim 1 further comprising forming at least one drain region close to the source region in the substrate.

3. The method of claim 1 further comprising smoothing the surface of the device by a Chemical-Mechanical Process.

4. The method of claim 1 wherein the second opening has a substantially uniform width.

5. The method of claim 1 wherein the removing further includes applying an isotropic dry-gas etching to pull back the floating gate layer under the second oxide layer.

6. A flash device comprising:

a first oxide layer on top of a substrate;

a floating gate layer on top of the first oxide layer;

a second oxide layer over the floating gate layer, wherein the second oxide layer and the floating gate layer have a first opening and a second opening respectively, and wherein the width of second opening is bigger than the width of the narrowest region of the first opening so that the floating gate layer is pulled back horizontally underneath the second oxide layer;

a source region in the substrate underneath the first oxide layer;

a third oxide layer filled in the first and second openings conforming to the contour thereof, wherein the third oxide has a third opening to reach a portion of the source region; and

a control gate material filling the third opening.

7. The device of claim 6 further comprising a drain region in the substrate wherein the source and drain regions, the floating gate layer, and the first oxide function collectively as a transistor.

8. The device of claim 6 wherein the surface of the device is smoothed by a Chemical-Mechanical Process.

9. The device of claim 6 wherein the second opening has a substantially uniform width.

10. The device of claim 6 wherein the second opening is of a predetermined width large enough to pull back the floating gate layer to avoid damages caused by ion implantation.

11. The device of claim 6 wherein an isotropic dry-gas etching is applied to pull back the floating gate under the second oxide.

12. A method for manufacturing a flash memory device, comprising:

forming a coupling oxide layer on top of a substrate;

forming a floating gate layer on top of the coupling oxide layer;

forming a dielectric barrier layer on top of the floating gate layer;

forming a shielding oxide layer over the floating gate layer and confined by the dielectric barrier layer;

removing a portion of the shielding oxide layer and the floating gate layer to form a first opening in the shielding oxide layer and a second opening in the floating gate layer, the first and second openings exposing a portion of the coupling oxide underneath the floating gate layer, the width of second opening being bigger than the width of the narrowest region of the first opening in the shielding oxide layer so that the shielding oxide layer shields the floating gate

layer and the coupling oxide layer underneath from being damaged;

forming a spacer oxide layer in the first and second openings, the spacer oxide layer conforming to a contour thereof;

removing a portion of the spacer oxide layer and the coupling oxide layer to make a third opening; and

depositing a control gate material through the third opening.

13. The method of claim 12 further comprising forming a source region in the substrate underneath the coupling oxide layer.

14. The method of claim 13 where in the source region is formed by ion implantation.

15. The method of claim 13 wherein the source region is formed before the spacer oxide layer is formed.

16. The method of claim 13 wherein the source region is formed after the third opening is made.

17. The method of claim 12 further comprising smoothing the surface of the device by a Chemical-Mechanical Process.

18. The method of claim 12 wherein the removing further includes applying an isotropic dry-gas etching to pull back the floating gate layer under the second oxide layer.

19. The method of claim 12 wherein the first opening has a sloped wall.

20. The method of claim 12 wherein the second opening has a substantially uniform width throughout.